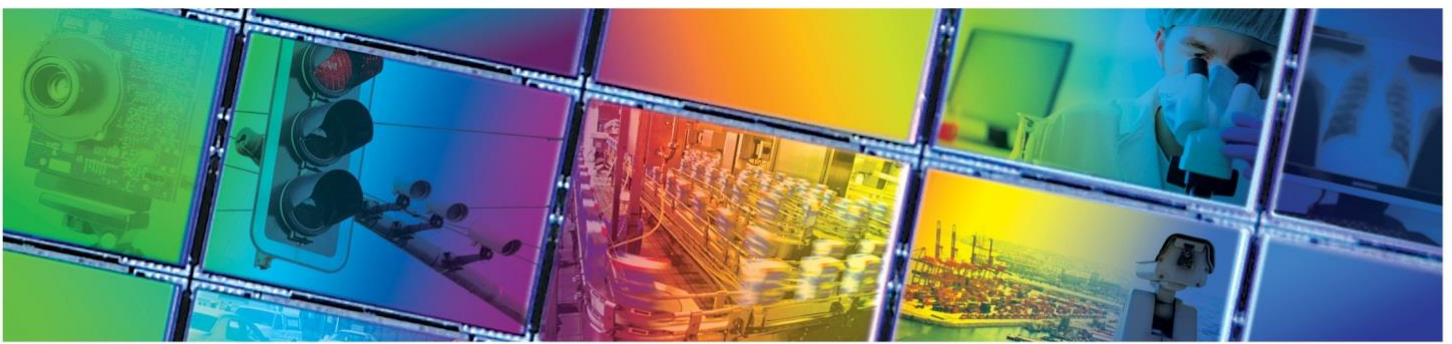


ON Semiconductor®



KAF-8300 IMAGE SENSOR

3326 (H) X 2504 (V) FULL FRAME CCD IMAGE SENSOR



JUNE 24, 2014

DEVICE PERFORMANCE SPECIFICATION

REVISION 1.1 PS-0029



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Summary Specification

KAF-8300 Image Sensor

DESCRIPTION

The KAF-8300 Image Sensor is a 22.5 mm diagonal (Four Thirds Format) high performance color or monochrome full frame CCD (charge-coupled device) image sensor designed for a wide range of image sensing applications including digital imaging. Each pixel contains blooming protection by means of a lateral overflow drain thereby preventing image corruption during high light level conditions. For the color version, the 5.4 μm square pixels are patterned with an RGB mosaic color filter with overlying microlenses for improved color response and reproduction. Several versions of monochrome devices are available with or without microlenses.

The sensor utilizes the TRUESENSE Transparent Gate Electrode to improve sensitivity compared to the use of a standard front side illuminated polysilicon electrode.

FEATURES

- TRUESENSE Transparent Gate Electrode for high sensitivity
- High Resolution
- High Dynamic Range
- Low Noise Architecture

APPLICATIONS

- Digitization
- Medical
- Scientific



Parameter	Typical Value
Architecture	Full Frame CCD; with Square Pixels
Total Number of Pixels	3448 (H) x 2574 (V) = approx. 8.9M
Number of Effective Pixels	
Color device	3358 (H) x 2536 (V) = approx. 8.6M
Monochrome device	3366 (H) x 2544 (V) = approx. 8.6M
Number of Active Pixels	3326 (H) x 2504 (V) = approx. 8.3M
Pixel Size	5.4 μm (H) x 5.4 μm (V)
Active Image Size	17.96 mm (H) x 13.52 mm (V) 22.5 mm (diagonal)
Aspect Ratio	4:3
Horizontal Outputs	1
Saturation Signal	> 25.5 ke ⁻
Output Sensitivity	23 $\mu\text{V}/\text{e}^-$
Quantum Efficiency, color R(600nm), G(540nm), B(480nm)	33%, 40 %, 33%
Quantum Efficiency, monochrome	
Microlens, clear glass (540 nm)	54%
Microlens, no glass (540 nm)	60%
Microlens, AR glass (540 nm)	56%
No Microlens, clear glass (560 nm)	37%
Total Sensor Noise	16 e ⁻
Dark Signal	< 200 e ⁻ /s
Dark Current Doubling Temperature	5.8 °C
Linear Dynamic Range	64.4 dB
Linearity Error at 12°C	± 10%
Charge Transfer Efficiency	0.999995
Blooming Protection (1ms integration time)	1000x saturation exposure
Maximum Data Rate	28 MHz
Package	32-pin CERDIP, 0.070" pin spacing
Cover Glass	Clear or AR coated, 2sides

Parameters above are specified at T = 60 °C and a data rate of 28 MHz unless otherwise noted



Ordering Information

Catalog Number	Product Name	Description	Marking Code
4H0827	KAF- 8300-AAB-CB-AA	Monochrome, No Microlens, CERDIP Package (sidebrazed), Clear Cover Glass (no coatings), Standard Grade	KAF-8300XE [Serial Number]
4H0828	KAF- 8300-AAB-CB-AE	Monochrome, No Microlens, CERDIP Package (sidebrazed), Clear Cover Glass (no coatings), Engineering Grade	
4H0927	KAF- 8300-AXC-CB-AA	Monochrome, Microlens, CERDIP Package (sidebrazed), Clear Cover Glass (no coatings), Standard Grade	KAF-8300-AXC [Serial Number]
4H0928	KAF- 8300-AXC-CB-AE	Monochrome, Microlens, CERDIP Package (sidebrazed), Clear Cover Glass (no coatings), Engineering Grade	
4H0929	KAF- 8300-AXC-CP-AA	Monochrome, Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass (no coatings), Standard Grade	KAF-8300-AXC [Serial Number]
4H0930	KAF- 8300- AXC-CP-AE	Monochrome, Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass (no coatings), Engineering Grade	
4H0944	KAF- 8300-AXC-CD-AA	Monochrome, Microlens, CERDIP Package (sidebrazed), Clear Cover Glass with AR coating (both sides), Standard Grade	KAF-8300-AXC [Serial Number]
4H0945	KAF- 8300- AXC-CD-AE	Monochrome, Microlens, CERDIP Package (sidebrazed), Clear Cover Glass with AR coating (both sides), Engineering Grade	
4H0469	KAF- 8300-CXB-CB-AA-Offset	Color (Bayer RGB), Special Microlens, CERDIP Package (sidebrazed), Clear Cover Glass (no coatings), Standard Grade, Offset	KAF-8300CE [Serial Number]
4H0468	KAF- 8300-CXB-CB-AE-Offset	Color (Bayer RGB), Special Microlens, CERDIP Package (sidebrazed), Clear Cover Glass (no coatings), Engineering Grade, Offset	
4H0471	KEK-4H0471-KAF- 8300-12-28	Evaluation Board (Complete Kit)	N/A

See Application Note *Product Naming Convention* for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.truesenseimaging.com.

Please address all inquiries and purchase orders to:

Truesense Imaging, Inc.
1964 Lake Avenue
Rochester, New York 14615

Phone: (585) 784-5500
E-mail: info@truesenseimaging.com

ON Semiconductor reserves the right to change any information contained herein without notice. All information furnished by ON Semiconductor is believed to be accurate.

Device Description

ARCHITECTURE

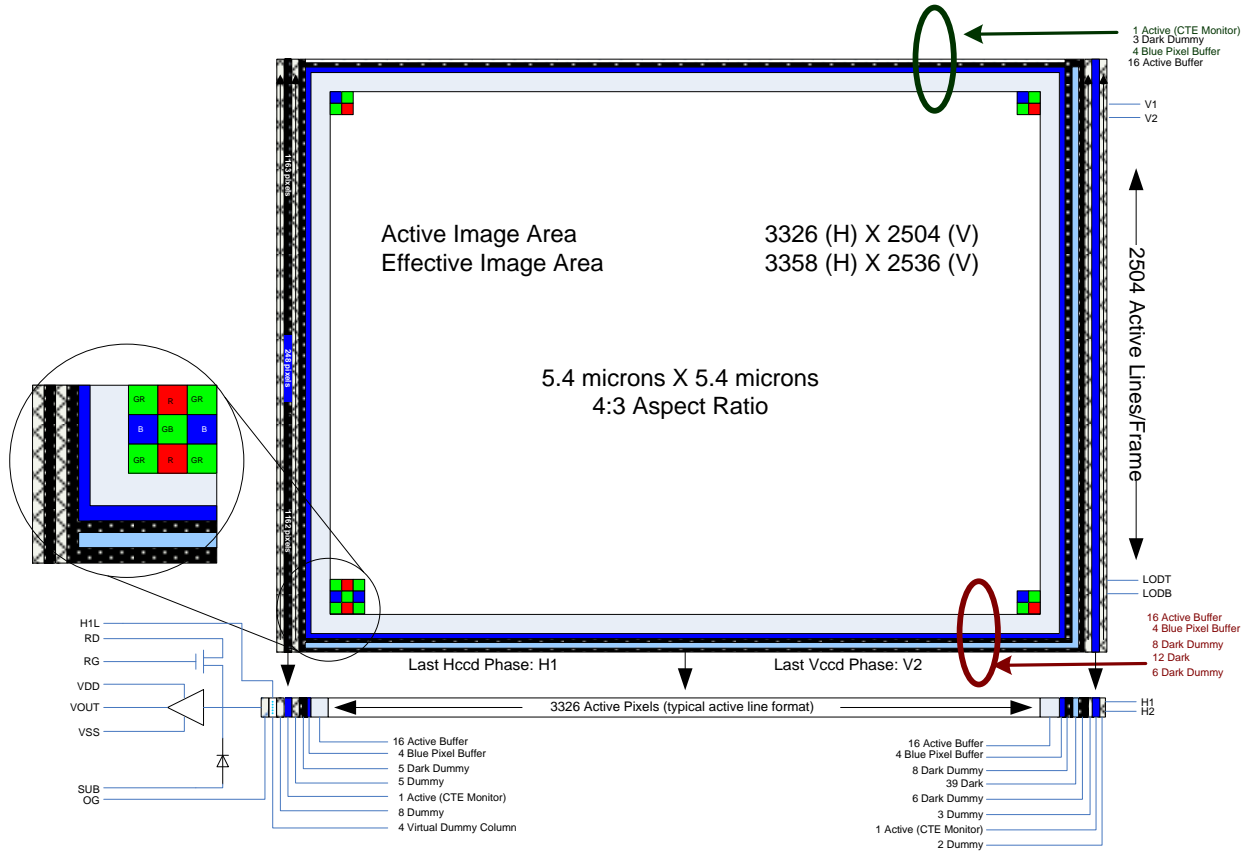


Figure 1: Block Diagram (color)

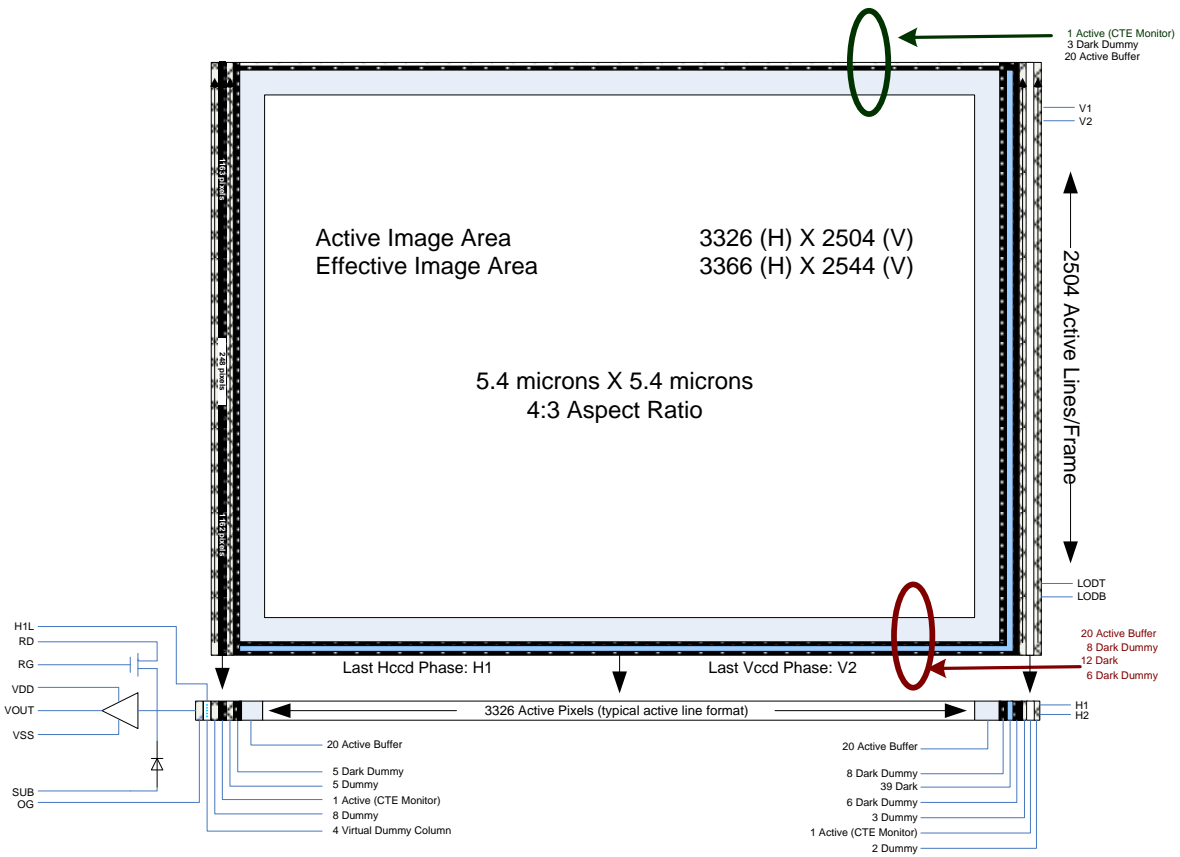


Figure 2: Block Diagram (monochrome)



Dark Reference Pixels

Surrounding the periphery of the device is a border of light shielded pixels creating a dark region. Within this dark region there are light shielded pixels that include 39 trailing dark pixels on every line. There are also 12 full dark lines at the start of every frame. Under normal circumstances, these pixels do not respond to light and may be used as a dark reference.

Dark Dummy Pixels

Within the dark region some pixels are in close proximity to an active pixel, or the light sensitive regions that have been added for manufacturing test purposes, (CTE Monitor). In both cases, these pixels can scavenge signal depending on light intensity and wavelength. These pixels should not be used as a dark reference. These pixels are called dark dummy pixels.

Within the dark region, dark dummy pixels have been identified. There are 5 leading and 14 (6 + 8) trailing dark pixels on every line. There are also 14 (6 + 8) dark dummy lines at the start of every frame along with 3 dark dummy lines at the end of each frame

Dummy Pixels

Within the horizontal shift register there are 13, (8 + 5), leading and 5, (2 + 3), trailing additional shift phases that are not electrically associated with any columns of pixels within the vertical register. These pixels contain only horizontal shift register dark current signal and do not respond to light and therefore, have been designated as dummy pixels. For this reason, they should not be used to determine a dark reference level.

Virtual Dummy Columns

Within the horizontal shift register there is 4 leading shift phases that are not physically associated with a column of pixels within the vertical register. These pixels contain only horizontal shift register dark current signal and do not respond to light and therefore, have been designated as virtual dummy columns. For this reason, they also should not be used to determine a dark reference level.

Active Buffer Pixels

For color devices, sixteen buffer pixels adjacent to the blue pixel buffer region contain a RGB mosaic color pattern. This region is classified as active buffer pixels. These pixels are light sensitive but they are not tested for defects and non-uniformities. The response of these pixels will not be uniform.

For monochrome devices, 20 buffer pixels adjacent to the dark dummy pixels are classified as active buffer pixels. These pixels are light sensitive but they are not tested for defects and non-uniformities. The response of these pixels will not be uniform.

Blue Pixel Buffer

For color devices, four buffer pixels adjacent to any leading or trailing dark reference regions contain a blue filter and is classified as a blue pixel buffer. These pixels are light sensitive but they are not tested for defects and non-uniformities. The response of these pixels will not be uniform.

Monochrome devices do not contain a blue pixel buffer.



CTE Monitor Pixels

Within the horizontal dummy pixel region two light sensitive test pixels (one each on the leading and trailing ends) are added and within the vertical dummy pixel region one light sensitive test pixel has been added. These CTE monitor pixels are used for manufacturing test purposes. In order to facilitate measuring the device CTE, the pixels in the CTE Monitor region in the horizontal and vertical portion is coated with blue pigment on the color version only. The monochrome device is uncoated).

IMAGE ACQUISITION

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the device. These photon-induced electrons are collected locally by the formation of potential wells at each photogate or pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons are discharged into the lateral overflow drain to prevent crosstalk or 'blooming'. During the integration period, the V1 and V2 register clocks are held at a constant (low) level.

CHARGE TRANSPORT

The integrated charge from each photogate is transported to the output using a two-step process. Each line (row) of charge is first transported from the vertical CCD's to a horizontal CCD register using the V1 and V2 register clocks. The horizontal CCD is presented a new line on the falling edge of V2 while H1 is held high. The horizontal CCD's then transport each line, pixel by pixel, to the output structure by alternately clocking the H1 and H2 pins in a complementary fashion. A separate connection to the last H1 phase (H1L) is provided to improve the transfer speed of charge to the floating diffusion. On each falling edge of H1 a new charge packet is dumped onto a floating diffusion and sensed by the output amplifier.

HORIZONTAL REGISTER

Output Structure

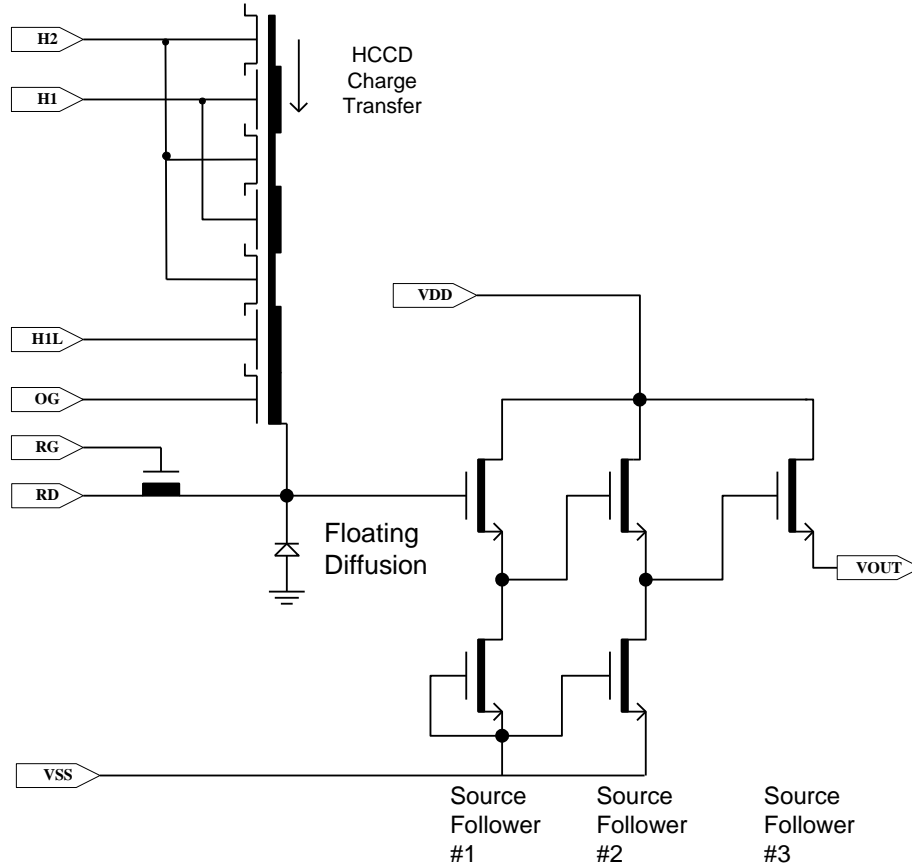


Figure 3: Output Architecture (Left or Right)

Charge presented to the floating diffusion (FD) is converted into a voltage and is current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on the FD. Once the signal has been sampled by the system electronics, the reset gate (RG) is clocked to remove the signal and FD is reset to the potential applied by reset drain (RD). Increased signal at the floating diffusion reduces the voltage seen at the output pin. To activate the output structure, an off-chip load must be added to the VOUT pin of the device. See Figure 4.



Output Load

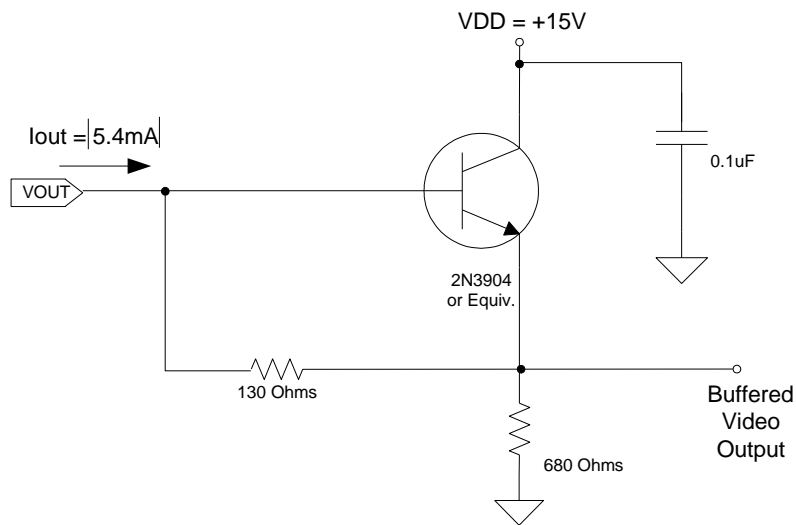


Figure 4: Recommended Output Structure Load Diagram

Note:

1. Component values may be revised based on operating conditions and other design considerations.



PHYSICAL DESCRIPTION

Pin Description and Device Orientation

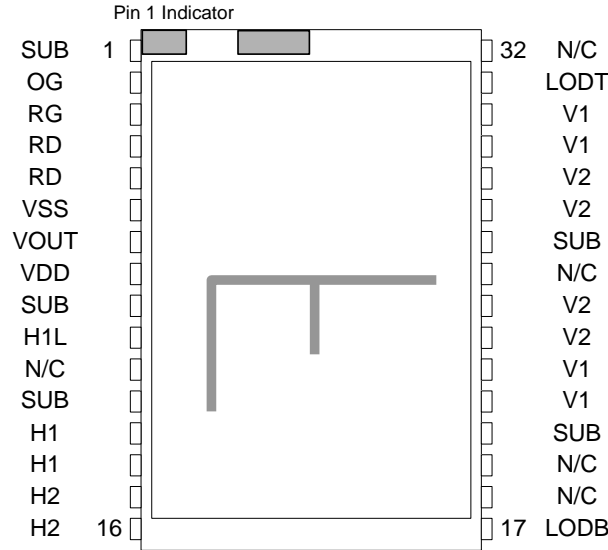


Figure 5: Pinout Diagram

Pin	Name	Description
1	SUB	Substrate
2	OG	Output Gate
3	RG	Reset Gate
4	RD	Reset Drain Bias
5	RD	Reset Drain Bias
6	VSS	Output Amplifier Return
7	VOUT	Output
8	VDD	Output Amplifier Supply
9	SUB	Substrate
10	H1L	Horizontal Phase 1, Last Gate
11	N/C	No Connection
12	SUB	Substrate
13	H1	Horizontal Phase 1
14	H1	Horizontal Phase 1
15	H2	Horizontal Phase 2
16	H2	Horizontal Phase 2

Pin	Name	Description
32	N/C	No Connection
31	LODT	Lateral Overflow Drain Top
30	V1	Vertical Phase 1
29	V1	Vertical Phase 1
28	V2	Vertical Phase 2
27	V2	Vertical Phase 2
26	SUB	Substrate
25	N/C	No Connection
24	V2	Vertical Phase 2
23	V2	Vertical Phase 2
22	V1	Vertical Phase 1
21	V1	Vertical Phase 1
20	SUB	Substrate
19	N/C	No Connection
18	N/C	No Connection
17	LODB	Lateral Overflow Drain Bottom

Note:

1. Wherever possible, all N/C pins (11, 18, 19, 25, 32) should be connected to GND (0V).



Imaging Performance

TYPICAL OPERATIONAL CONDITIONS

Description	Condition - Unless otherwise noted	Notes
Readout Time (t_{readout})	370.36 msec	Includes $t_{\text{Voverclock}}$ & $t_{\text{Hoverclock}}$
Integration time (t_{int})	33 msec	
Horizontal clock frequency	28 MHz	
Light source (LED)	Red, green, blue, orange	
Mode	Flush – integrate – readout cycle	

SPECIFICATIONS

All Devices

Description	Symbol	Min.	Nom.	Max	Units	Notes	Verification Plan
Minimum Column	MinColumn	575			mV	1, 4	die ¹⁸
Linear Saturation Signal	Ne_{sat}	25.5K			e^-	1, 3, 4	design ¹⁹
Charge to Voltage Conversion	Q-V	22.5	23		$\mu\text{V}/e^-$		design ¹⁹
Linearity Error	LeLow10	-10		10	%	2, 5, 6	die ¹⁸
	LeLow33	-10		10	%	2, 5, 6	die ¹⁸
	LeHigh	-10		10	%	2, 5, 4	die ¹⁸
Dark Signal (Active Area Pixels)	AA_DarkSig			200	e^-/s	4, 8	die ¹⁸
Dark Signal (Dark Reference Pixels)	DR_DarkSig			200	e^-/s	4, 8	die ¹⁸
Readout Cycle Dark Signal	Dark_Read			15	mV/s		die ¹⁸
Flush Cycle Dark Signal	Dark_Flush		43	90	mV/s		die ¹⁸
Dark Signal Non-Uniformity	DSNU		1.30	3	mVp-p	4, 9	die ¹⁸
	DSNU_Step		0.14	0.5	mV p-p	4, 9	die ¹⁸
	DSNU_H		0.4	1.0	mVp-p	4, 9	die ¹⁸
Dark Signal Doubling Temperature	ΔT		5.8		$^{\circ}\text{C}$		design ¹⁹
Dark Reference Difference, Active Area	DarkStep	-3.5	0.15	3.5	mV	4	die ¹⁸
Total Noise	DfId_noi			1.08	mV	4, 10	die ¹⁸
Total Sensor Noise	N		16		e^-_{rms}	19	design ¹⁹
Linear Dynamic Range	DR		64.4		dB	11	design ¹⁹
Horizontal Charge Transfer Efficiency	HCTE	0.999990	0.999995			4, 13, 21	die ¹⁸
Vertical Charge Transfer Efficiency	VCTE	0.99997	0.999999		%	4, 21	die ¹⁸
Blooming Protection	X_b	1000			$x \text{ Esat}$	14	design ¹⁹
Vertical Bloom on Transfer	VBloomF	-20		20	mV	4	die ¹⁸
Horizontal Crosstalk	H_Xtalk	-20		20	mV	4	die ¹⁸
Horizontal Overclock Noise	Hoclk_noi	0		1.08	mV	4	die ¹⁸
Output Amplifier Bandwidth	$f_{-3\text{dB}}$	88		159	Mhz	4, 6, 16	die ¹⁸
Output Impedance, Amplifier	R _{OUT}	100		180	Ohms	6	die ¹⁸
Hclk Feedthru	V _{hft}			70	mV	4, 17	die ¹⁸
Reset Feedthru	V _{rft}	500	710	1000	mV		design ¹⁹



Color Devices

Description	Symbol	Min.	Nom.	Max	Units	Notes	Verification Plan
Sensitivity red green blue	Rresp Gresp Bresp	260 442 230		420 638 420	mV mV mV		die ¹⁸ die ¹⁸ die ¹⁸
QE R(600nm) G(540nm) B(480nm)	QE, red QE green QE, blue		33 40 33		%		design ¹⁹
Off-band Response Green inband Red response Blue response Red inband Green response Blue response Blue inband Red response Green response	Gr_Gresp Gr_Rresp Gr_Bresp Rd_Rresp Rd_Gresp Rd_Bresp Bl_Bresp Bl_Rresp Bl_Gresp	362 0 0 180 0 0 90 0 0		630 130 260 430 120 45 420 40 120	mV mV mV mV mV mV mV mV mV		die ¹⁸ die ¹⁸ die ¹⁸ die ¹⁸ die ¹⁸ die ¹⁸ die ¹⁸ die ¹⁸ die ¹⁸
Linearity Balance	Red_Bal Blu_Bal	-14 -8	6.4 0.2	14 8	% %	2, 6 2, 6	die ¹⁸ die ¹⁸
Photo Response Non-Uniformity	R_PRNU G_PRNU B_PRNU			15 15 15	%p-p %p-p %p-p	7 7 7	die ¹⁸ die ¹⁸ die ¹⁸
High Frequency Noise	R_Nois GRr_Nois GBr_Nois B_Nois			2 2 2 2	%rms %rms %rms %rms		die ¹⁸ die ¹⁸ die ¹⁸ die ¹⁸
Red-Green Hue Shift	RGHueUnif			10	%	12	die ¹⁸
Blue-Green Hue Shift	BGHueUnif			12	%	12	die ¹⁸
GRr/GBr Hue Uniformity	GrGbHueUnf			7	%	12	die ¹⁸
Green Light GRr/GBr Hue Uniformity	Gr_GHueUnf			9	%		die ¹⁸
Low Hue Uniformity	RGLoHueUnf BGLoHueUnf			12 10	% %		die ¹⁸ die ¹⁸
Streak/Spot	GrnStreak RedStreak BluStreak			40 20 20	% % %		
Local Green Difference white light, min white light, max green light, min green light, max red light, min red light, max blue light, min blue light, max	W_GNU_Min W_GNU_Max Gr_GNU_Min Gr_GNU_Max R_GNU_Min R_GNU_Max B_GNU_Min B_GNU_Max			4 6 4 4 65 65 40 40	% % % % % % % %		die ¹⁸ die ¹⁸ die ¹⁸ die ¹⁸ die ¹⁸ die ¹⁸ die ¹⁸ die ¹⁸
Chroma Test	UL_Chroma UR_Chroma LL_Chroma LR_Chroma			7 7 7 7	% % % %		die ¹⁸ die ¹⁸ die ¹⁸ die ¹⁸
Hue Test	UL_UR_Hue UL_LR_Hue UL_LL_Hue UR_LR_Hue UR_LL_Hue LR_LL_Hue			6 6 6 6 6 6	% % % % % %		die ¹⁸ die ¹⁸ die ¹⁸ die ¹⁸ die ¹⁸ die ¹⁸



Monochrome Versions Only

Description	Symbol	Min.	Nom.	Max	Units	Notes	Verification Plan
Sensitivity Monochrome	Resp	465		655	mV		die ¹⁸
QE Microlens, clear glass (540 nm) Microlens, no glass (540 nm) Microlens, AR glass (540 nm) No Microlens, clear glass (560 nm)	QE		54% 60% 56% 37%		%		design ¹⁹

Notes:

- Increasing output load currents to improve bandwidth will decrease these values.
- Specified from 12 °C to 60 °C.
- Saturation signal level achieved while meeting Le specification. Specified from 0 °C to 40 °C.
- Operating temperature = 60 °C.
- Worst case deviation, (from 10 mV to Vsat min), relative to a linear fit applied between 0 and 500 mV exposure.
- Operating temperature = 25 °C.
- Peak to peak non-uniformity test based on an average of 185 x 185 blocks.
- Average non-illuminated signal with respect to over clocked horizontal register signal.
- Absolute difference between the maximum and minimum average signal levels of 185 x 185 blocks within the sensor.
- Dark rms deviation of a multi-sampled pixel as measured using the KAF-8300 Evaluation Board.
- $20\log(V_{sat}/N)$
- Gradual variations in hue (red with respect to green pixels and blue with respect to green pixels) in regions of interest of 185 x 185 blocks.
- Measured per transfer at 80% of Vsat.
- Esat equals the exposure required to achieve saturation. X_b represents the number of Esat exposures the sensor can tolerate before failure. X_b characterized at 25 °C.
- Video level DC offset with respect to ground at clamp position. Refer to Figure 16.
- Last stage only. CLOAD = 10pF. Then $f_{-3dB} = (1 / (2\pi * R_{OUT} * CLOAD))$.
- Amount of artificial signal due to H1 coupling.
- A parameter that is measured on every sensor during production testing.
- A parameter that is quantified during the design verification activity.
- Calculated value subtracting the noise contribution from the KAF-8300 Evaluation Board.
- Process optimization has effectively eliminated vertical striations.
- $CTE = 1 - CTI$. Where CTE is charge transfer efficiency and CTI is charge transfer inefficiency. CTI is the measured value.



Typical Performance Curves

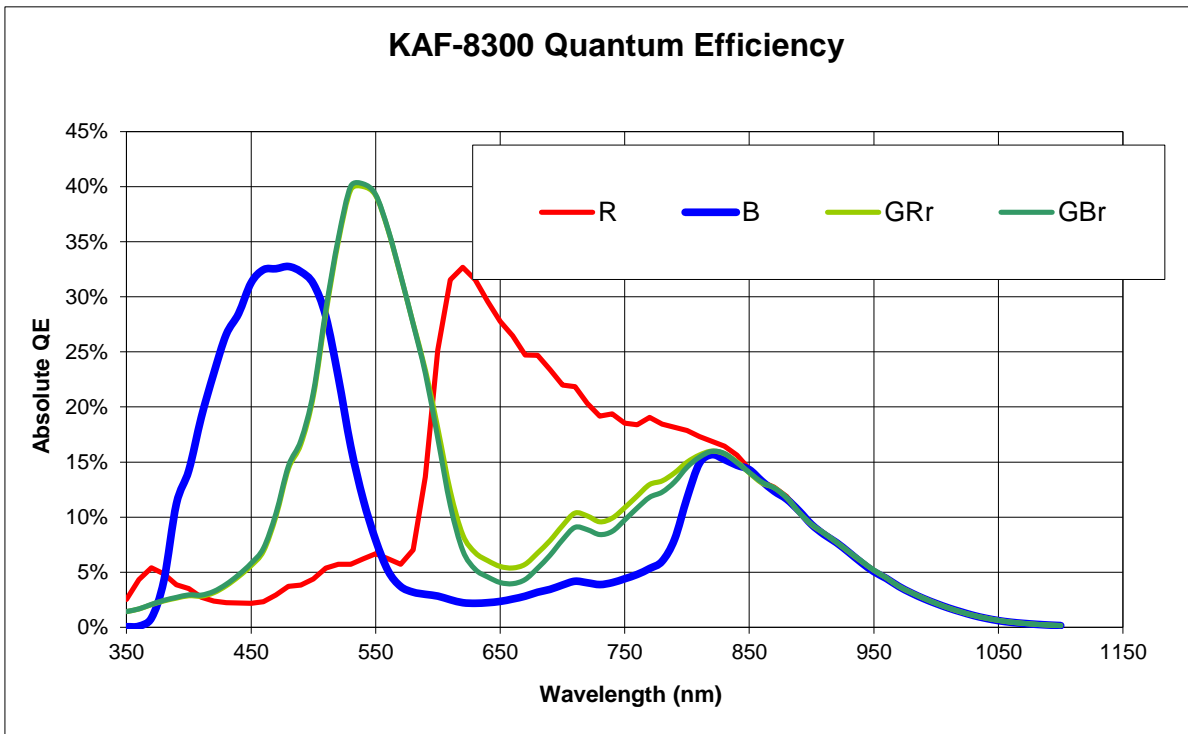


Figure 6: Typical Quantum Efficiency, Color version

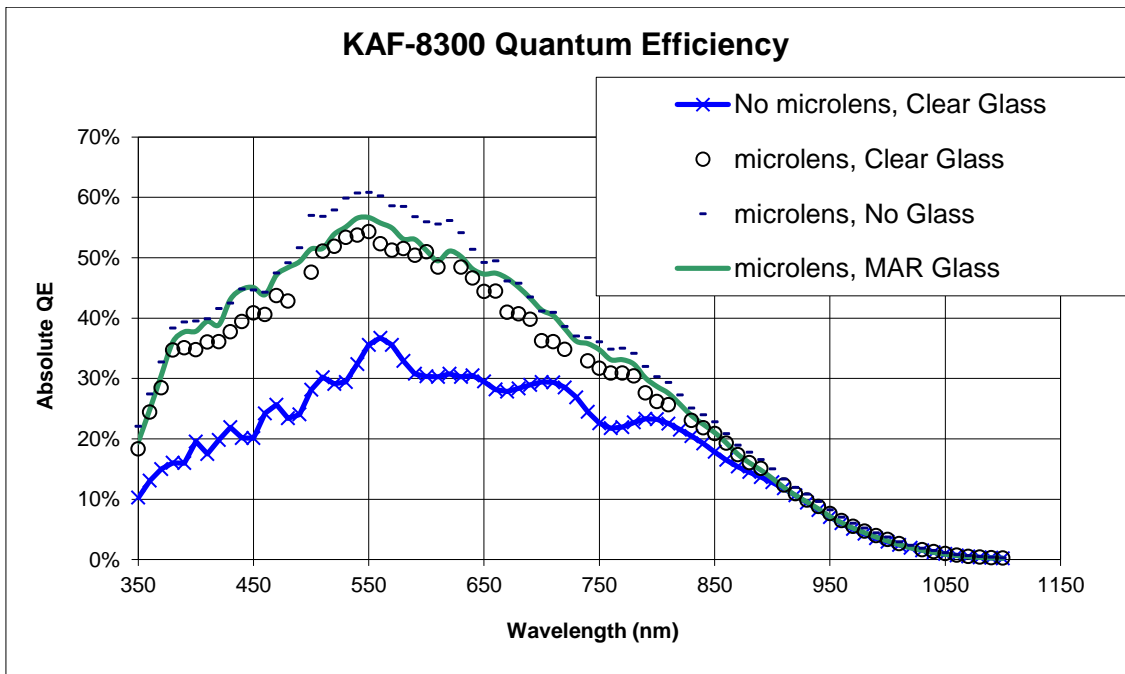


Figure 7: Typical Quantum Efficiency, all Monochrome versions

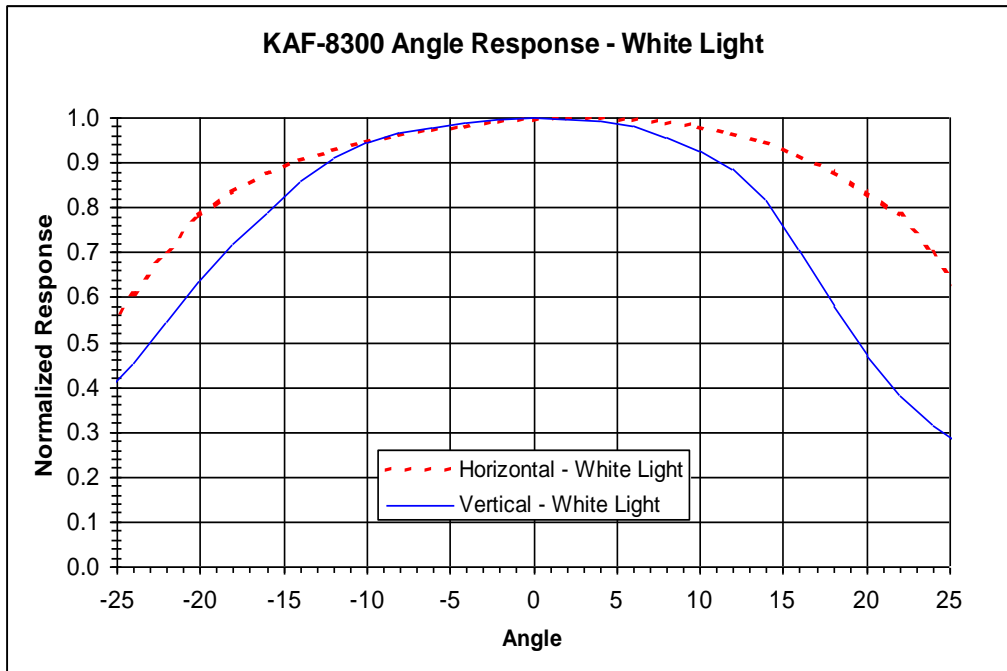


Figure 8: Typical Angular Response, Color version

Note:

1. The center location of the die is as shown. The effective optical shift is 6° center-to-edge, along the diagonal.

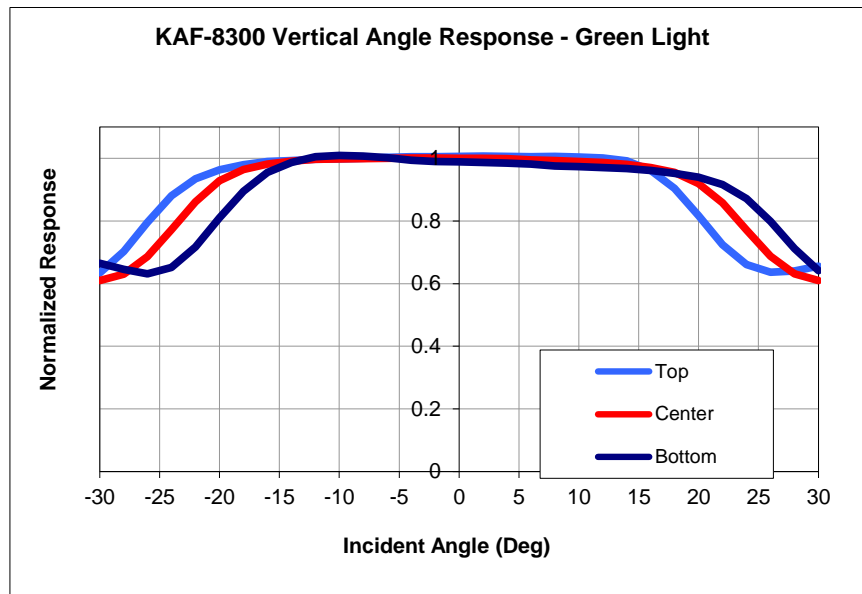


Figure 9: Typical Angular Response, Monochrome with microlens

Note:

1. The effective optical shift is 6° center-to-edge, along the diagonal.



Defect Definitions

OPERATIONAL CONDITIONS

The Defect Specifications are measured using the following conditions:

Description	Test Condition	Notes
Integration time (tint)	33 msec	Unless otherwise noted

SPECIFICATIONS

All Devices

Description	Symbol	Definition	Threshold	Maximum Number Allowed	Notes
Point defect	BPnt33_7	Dark field, minor, short integration time	7.5 mV	800 total Points allowed for this group of tests	3
Point defect	Bfld_Pnt_D	Dark point in an illuminated field	11%		3
Point defect	Bfld_Pnt_B	Bright point in an illuminated field	7%		3
Point defect	BPnt33_100	Dark field, major, short integration time	100 mV		3
Point defect	BPnt33_500	Dark field, major, short integration time	500 mV	0	3
Point defect	BPnt333_13	Dark field, minor, long integration time, tint=1/3 sec	13 mV	32,500	1, 3, 4
Point Defect	DR_BPnts	Bright point in the dark reference region	7.5 mV	0	5
Cluster defect	Total_Clst	A cluster is a group of 2 or more defective pixels that do not exceed the perpendicular pattern defect.	---	6 total	3
Cluster defect	Dfld_Vperp	Dark field very long exposure bright cluster where 9 or more adjacent point defects exist, very long integration time, tint=1 sec	3.04 mV	0	3
Cluster Defect – Perpendicular Pattern Defect	Dfld_Perp Bfld_Perp Total_Perp	Three or more adjacent point defects in the same color plane, along a row or column.	---	0	2, 3
Column defect, illuminated	Bfld_Col_D Bfld_Col_B	A column which deviates above or below neighboring columns under illuminated conditions (>300mV signal) greater than the threshold	1.5% 1.5%	0	3
Column defect, darkfield	Dfld_Col2	A column which deviates above or below neighboring columns under non-illuminated or low light level conditions (~10mV) greater than the threshold	1 mV	0	3
	Dfld_Col4		1 mV		3
	Lo_Col_B		1 mV		5
	Lo_Col_D		1 mV		5
	Lo_Col_B1 Lo_Col_D1		1 mV 1 mV		5 5
Row Defect	Dfld_Row	Row defect if row average deviates above threshold	1 mV	0	3
LOD Bright Col, dark	Dfld_LodCol	Defines functionality and uniform efficiency of LOD structure	1.5 mV	0	3



Color Devices

Description	Symbol	Definition	Threshold	Maximum Number Allowed
Streak Test, color	GrnStreak RedStreak BluStreak	Maximum defect density gradient allowed in a color bit plane. ⁴	40% 20% 20%	0

Notes:

1. This parameter is only a quality metric and these points will not be considered for cluster and point criteria.
2. For the color version of this device, the green pixels in a red row (GR) are considered a different color plane than the green pixels in a blue row (GB). For monochrome version the entire active area is treated as a single color plane.
3. Operating temperature = 60 °C.
4. As the gradient threshold is defined as 8.5 mV maximum across a 16 x 16 pixel region about each pixel.
5. Operating temperature = 25 °C.



Operation

Absolute Maximum Ratings

Description ⁹	Symbol	Minimum	Maximum	Units	Notes
Diode Pin Voltages	V_{diode}	-17.5	+17.5	V	1, 2
Gate Pin Voltages	V_{gate1}	-13.5	+13.5	V	1, 3
Overlapping Gate Voltages	V_{1-2}	-13.5	+13.5	V	4
Non-overlapping Gate Voltages	V_{g-g}	-13.5	+13.5	V	5
V1, V2 – LOD Voltages	V_{VL}	-13.5	+13.5	V	6
Output Bias Current	I_{out}		-30	mA	7
LODT Diode Voltage	V_{LODT}	-13.0	+13.0	V	8
LODB Diode Voltage	V_{LODB}	-18.0	+18.0	V	8
Operating Temperature	T_{OP}	-10	70	°C	10
Guaranteed Temperature of Performance	T_{SP}	0	60	°C	11

Notes:

1. Referenced to pin SUB
2. Includes pins: RD, VDD, VSS, and VOUT.
3. Includes pins: V1, V2, H1, H1L, H2, RG, OG.
4. Voltage difference between overlapping gates. Includes: V1 to V2; H1, H1L to H2; H1L to OG; V1 to H2.
5. Voltage difference between non-overlapping gates. Includes: V1 to H1, H1L; V2, OG to H2.
6. Voltage difference between V1 and V2 gates and LODT, LODB diode.
7. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher currents and lower load capacitance at the expense of reduced gain (sensitivity). Operation at these values will reduce MTF.
8. V1, H1, V2, H2, H1L, OG, and RD are tied to 0V.
9. Absolute maximum rating is defined as a level or condition that should not be exceeded at any time per the description. If the level or condition is exceeded, the device will be degraded and may be damaged.
10. Noise performance will degrade at higher temperatures.
11. See section for Imaging Performance Specifications.

POWER-UP SEQUENCE

The sequence chosen to perform an initial power-up is not critical for device reliability. A coordinated sequence may minimize noise and the following sequence is recommended:

1. Connect the ground pins (SUB).
2. Supply the appropriate biases and clocks to the remaining pins.



DC BIAS OPERATING CONDITIONS

Description	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current (mA)	Notes
Reset Drain	RD	11.3	11.5	11.7	V	$I_{RD} = 0.01$	
Output Amplifier Return	VSS	1.05	1.25	1.45	V	$ISS = -3.0$	
Output Amplifier Supply	VDD	14.5	15.0	15.5	V	$I_{OUT} + ISS$	
Substrate	SUB		GND		V	-0.01	2
Output Gate	OG	-3	-2.8	-2.6	V	0.1	
Lateral Drain	LODT, LODB	9.5	9.75	10.0	V	0.2	2
Video Output Current	I_{OUT}	-3	-5	-8	mA		1

Notes:

1. An output load sink must be applied to VOUT to activate output amplifier – see Figure 4.
2. Maximum current expected up to saturation exposure (E_{sat}).

AC OPERATING CONDITIONS

Clock Levels

Description	Symbol	Level	Minimum	Nominal	Maximum	Units	Effective Capacitance	Notes
V1 Low Level	V1L	Low	-9.5	-9.25	-9.0	V	76 nF	1
V1 High Level	V1H	High	2.4	2.6	2.85	V		1
V2 Low Level	V2L	Low	-9.5	-9.25	-9.0	V	81 nF	1
V2 High Level	V2H	High	2.4	2.6	2.8	V		1
RG, H1, H2, amplitude	RGamp H1amp H2amp	Amp	5.5	6.0	6.5	V	RG = 7 pF H1 = 224 pF H2 = 168 pF	1
H1L, amplitude	H1Lamp	Amp	7.5	8.0	8.5	V	7 pF	1
H1 Low Level	H1low	Low	-4.7	-4.5	-4.3	V		1
H1L Low Level	H1Llow	Low	-6.7	-6.5	-6.3	V		
H2 Low Level	H2low	Low	-5.2	-5	-4.8	V		
RG Low Level	RG low	Low	1.8	2.0	2.2	V		1

Note:

1. All pins draw less than 10 mA DC current. Capacitance values relative to SUB (substrate).



Clock Voltage Detail Characteristics

Description	Symbol	Min	Nom	Max	Units	Notes
V1 High-level variation	V1 _{HH}	-	0.50	1	V	High-level coupling
V2 High-level variation	V2 _{HL}	-	0.28	1	V	High-level coupling
V2 Low-level variation	V2 _{LH}	-	0.46	1	V	Low-level coupling
V1 Low-level variation	V1 _{LL}	-	0.14	1	V	Low-level coupling
V1-V2 Cross-over	V1 _{CR}	-2	-0.5	1	V	Referenced to ground
H1 High-level variation	H1 _{HH}	-	0.30	1	V	
H1 High-level variation	H1 _{HL}	-	0.07	1	V	
H1 Low-level variation	H1 _{LH}	-	0.16	1	V	
H1 Low-level variation	H1 _{LL}	-	0.25	1	V	
H2 High-level variation	H2 _{HH}	-	0.40	1	V	
H2 High-level variation	H2 _{HL}	-	0.06	1	V	
H2 Low-level variation	H2 _{LH}	-	0.10	1	V	
H2 Low-level variation	H2 _{LL}	-	0.27	1	V	
H1 – H2 Cross-over	H1 _{CR1}	-3	-1.23	0	V	Rising side of H1
H1 – H2 Cross-over	H1 _{CR2}	-3	-0.59	0	V	Falling side of H1
H1L High-level variation	H1 _{LHH}	-	0.64	1	V	
H1L High-level variation	H1 _{LHL}	-	0.32	1	V	
H1L Low-level variation	H1 _{L LH}	-	0.27	1	V	
H1L Low-level variation	H1 _{LLL}	-	0.23	1	V	
H1L – H2 Cross-over	H1 _{LCR1}	-1	-	-3	V	Rising side of H1L
RG High-level variation	RG _{HH}	-	0.19	1	V	
RG High-level variation	RG _{HL}	-	0.20	1	V	
RG Low-level variation	RG _{LH}	-	0.11	1	V	
RG Low-level variation	RG _{LL}	-	0.30	1	V	

Notes:

1. H1, H2 clock frequency: 28 MHz. The maximum and minimum values in this table are supplied for reference. The actual clock levels were measured using the KAF-8300 Evaluation Board. Testing against the device performance specifications is performed using the nominal values.



CAPACITANCE EQUIVALENT CIRCUIT

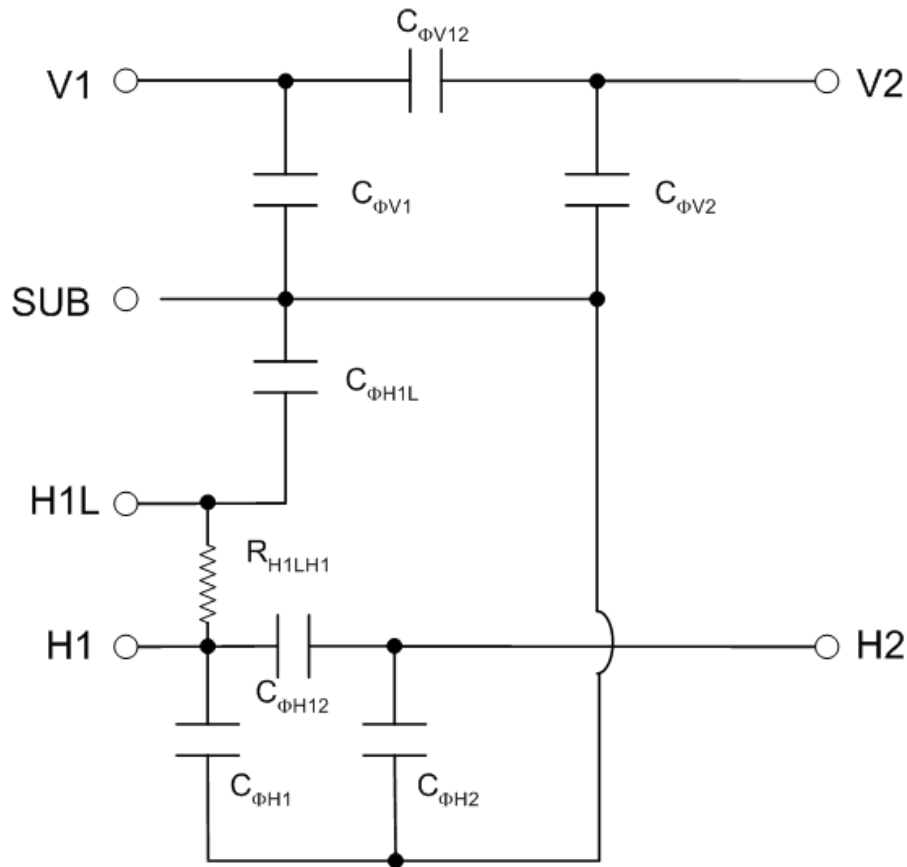


Figure 10: Equivalent Circuit Model

Note:

1. The external pin names are actual pins on this image sensor. See the pinout diagram (Figure 5) for more information.
2. The components shown in this schematic model do not correspond to actual components inside the image sensor.

Parameter	Value (typical)	Units
$C_{\phi V1}$	61	nF
$C_{\phi V12}$	15	nF
$C_{\phi V2}$	67	nF
$C_{\phi H1}$	153	pF
$C_{\phi H12}$	36	pF
$C_{\phi H2}$	97	pF
$C_{\phi H1L}$	7	pF
R_{H1LH1}	52	Kohms



Timing

REQUIREMENTS AND CHARACTERISTICS

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
H1, H2 Clock Frequency	f_H			28	MHz	1, 2
V1, V2 Clock Frequency	f_V			125	kHz	2
Pixel Period (1 Count)	t_e	35.7			ns	2
H1, H2 Setup Time	t_{HS}	1			μ s	
H1L – VOUT Delay	t_{HV}		3		ns	
RG – VOUT Delay	t_{RV}		1		ns	
Readout Time	$t_{readout}$	340.2			ms	4, 5
Integration Time	t_{int}					3, 4
Line Time	t_{line}	132.2			ms	4
Flush Time	t_{flush}	21.23			ms	6

Notes:

1. 50% duty cycle values.
2. CTE will degrade above the nominal frequency.
3. Integration time is user specified.
4. Longer times will degrade noise performance.
5. $t_{readout} = t_{line} * 2574$ lines.
6. See Figure 18 for a detailed description.

Clock Switching Characteristics

Description	Symbol	Min	Nom	Max	Units	Notes
V1 Rise Time	t_{V1r}	-	0.26	1	μ s	3
V2 Rise Time	t_{V2r}	-	0.55	1	μ s	3
V1 Fall Time	t_{V1f}	-	0.43	1	μ s	3
V2 Fall Time	t_{V2f}	-	0.31	1	μ s	3
V1 Pulse Width	t_{V1w}	5.0	-	-	μ s	4, 5
V2 Pulse Width	t_{V2w}	3.0	-	-	μ s	4, 5
H1 Rise Time	t_{H1r}	-	9.0	10	ns	3
H2 Rise Time	t_{H2r}	-	6.9	10	ns	3
H1 Fall Time	t_{H1f}	-	5.8	10	ns	3
H2 Fall Time	t_{H2f}	-	5.4	10	ns	3
H1 – H2 Pulse Width	t_{H1w}, t_{H2w}	14	18	22	ns	
H1L Rise Time	t_{H1Lr}		1.8	4	ns	3
H1L Fall Time	t_{H1Lf}		2.5	4	ns	3
H1L Pulse Width	t_{H1Lw}	14	19.0	22	ns	
RG Rise Time	t_{RGr}	-	2.0	4	ns	3
RG Fall Time	t_{RGf}	-	2.2	4	ns	3
RG Pulse Width	t_{RGw}	-	6.7	-	ns	2

Notes:

1. H1, H2 clock frequency: 28 MHz. The maximum and minimum values in this table are supplied for reference. The actual clock timing was measured using the KAF-8300 Evaluation Board. Testing against the device performance specifications is performed using the nominal values.
2. RG should be clocked continuously.
3. Relative to the pulse width (based on 50% of high/low levels).
4. CTE
5. Longer times will degrade noise performance.



EDGE ALIGNMENT

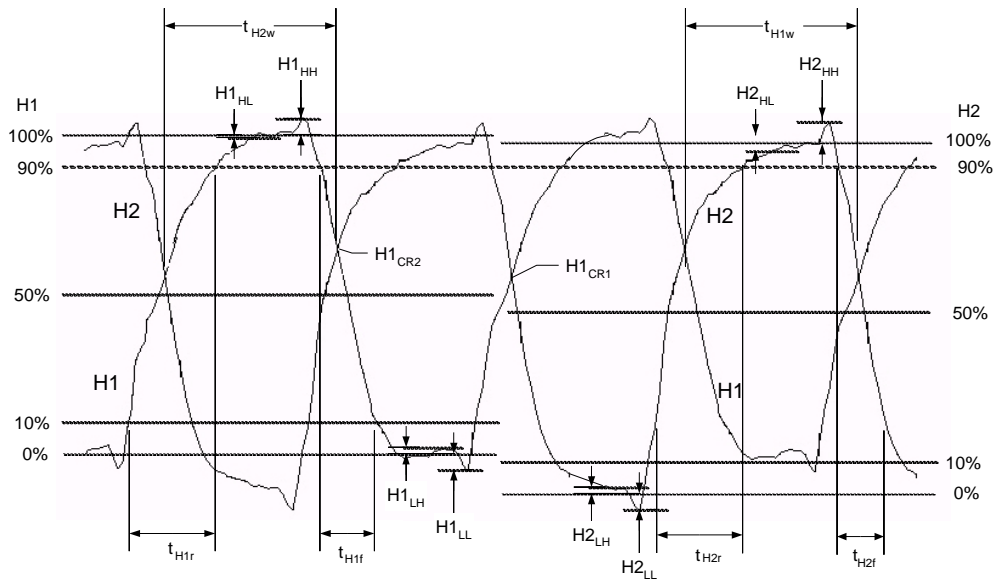


Figure 11: H1 and H2 Edge Alignment

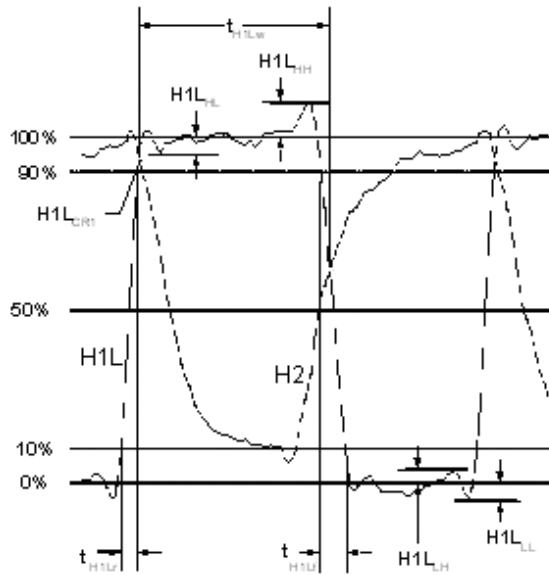


Figure 12: H1L and H2 Edge Alignment



FRAME TIMING

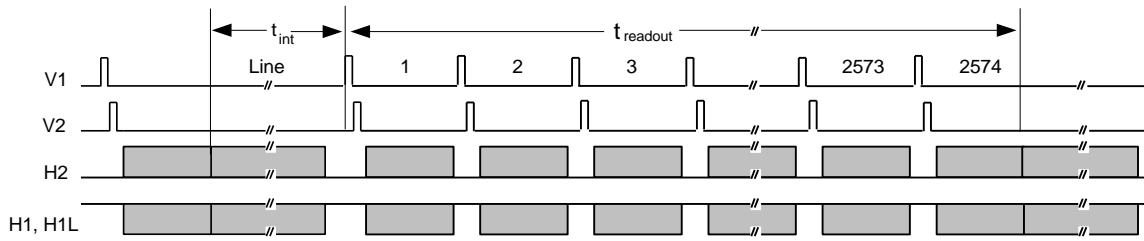


Figure 13: Frame Timing (minimum)

Frame Timing Detail

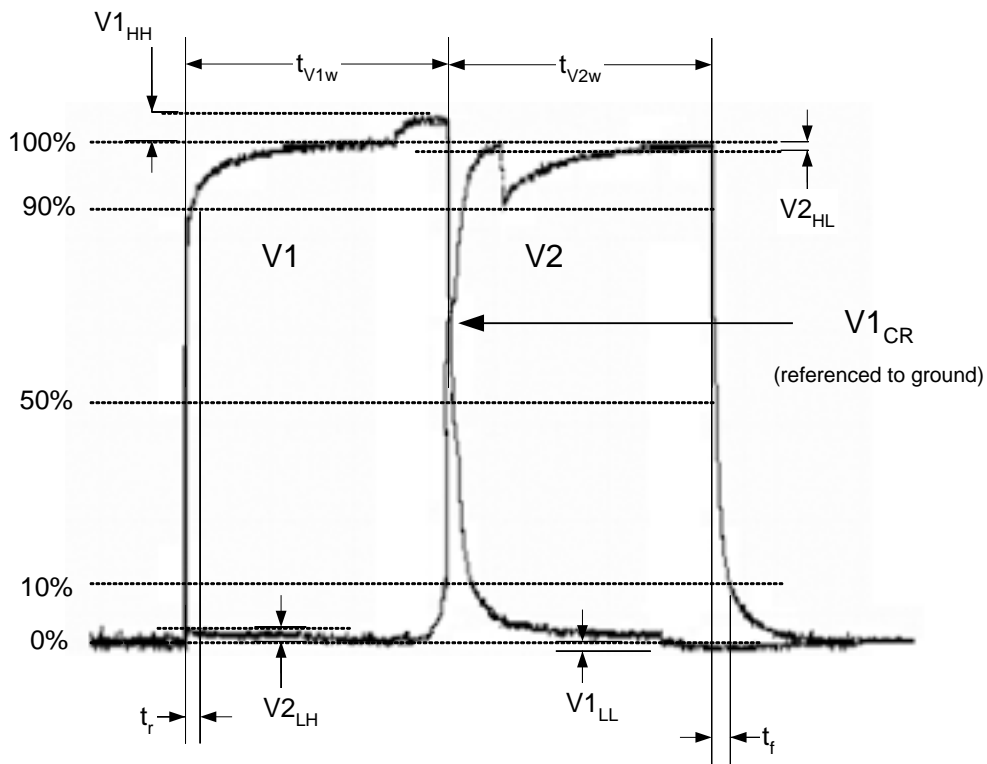
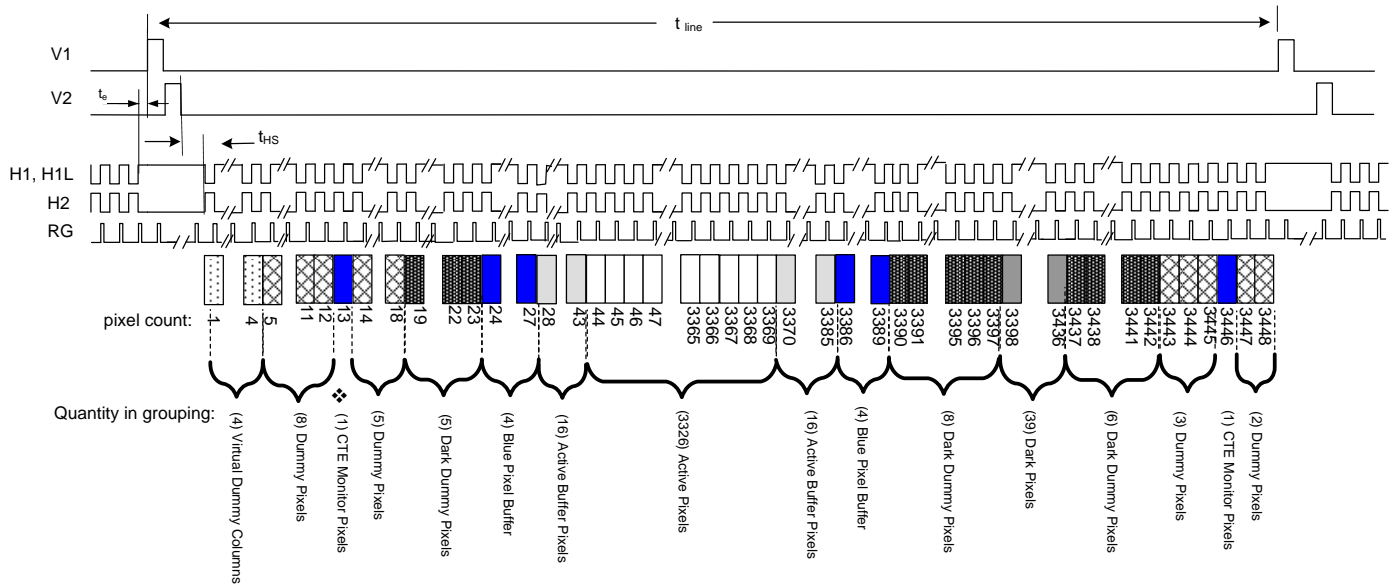


Figure 14: Frame Timing Edge Alignment



LINE TIMING



KAF-8300 has 2574 lines (rows) in a single frame.
 Line shown above represents the device output for lines 1164-1411 only.

The device output for the other lines are detailed below:

- **** Lines 27 - 30 and 2551 - 2554 are lines mostly composed of blue photoactive buffer pixels.
 - ** Lines 31 - 46 and 2555 - 2570 are lines mostly composed of photoactive buffer pixels.
 - * Lines 7-18 are lines mostly composed of dark reference pixels.
 - *** Lines 1 - 6, 19-26, and 2571 - 2574 are lines mostly composed of dark dummy pixels and are not to be used for imaging purposes or as a dark reference.
-
- ❖ For lines 1412 thru 2570 are as shown above with the following exception: pixel 13 are denoted as a dark dummy pixels for these lines.
 - ❖ For lines 1 thru 1163 are as shown above with the following exception: pixel 13 are denoted as a test pixel, of which all are dark dummy except for one photoactive pixel for which row location may vary.

Figure 15: Line Timing

Note:

1. Schematic reference regions that contain a blue filter represent the color version only; monochrome version is uncoated for these pixels.



PIXEL TIMING

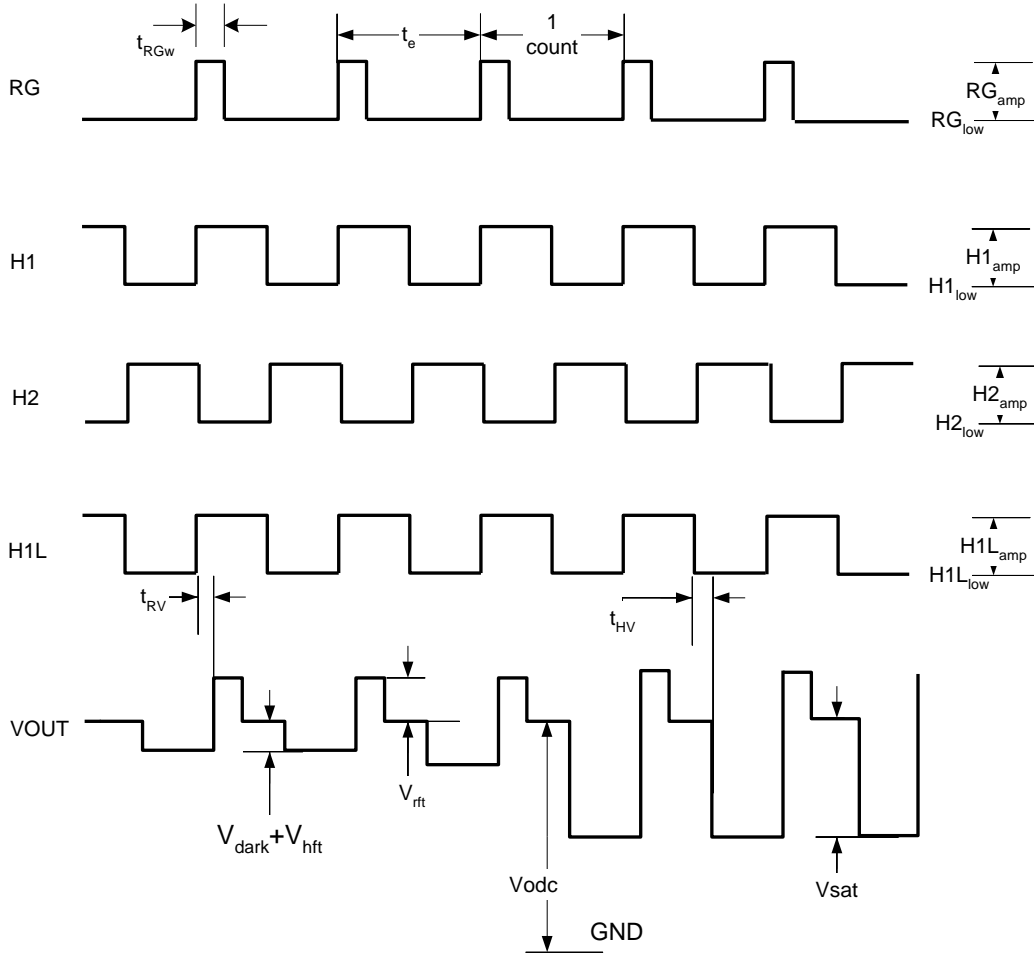


Figure 16: Pixel Timing



Pixel Timing Detail

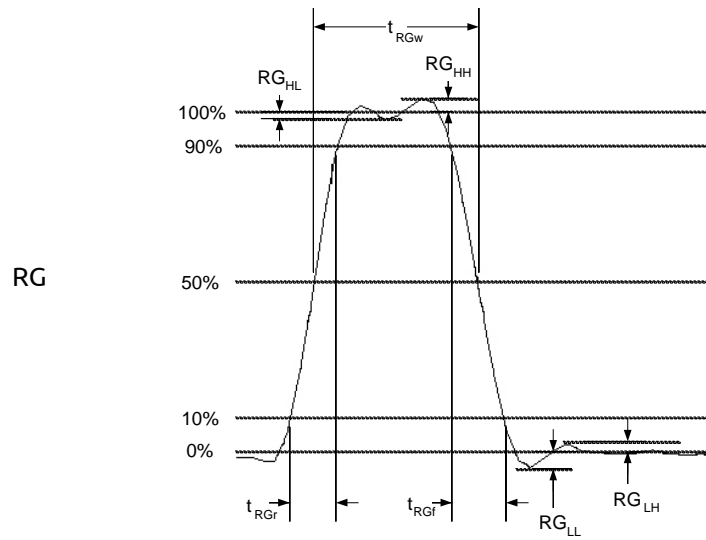


Figure 17: Pixel Timing Detail



Mode of Operation

POWER-UP FLUSH CYCLE

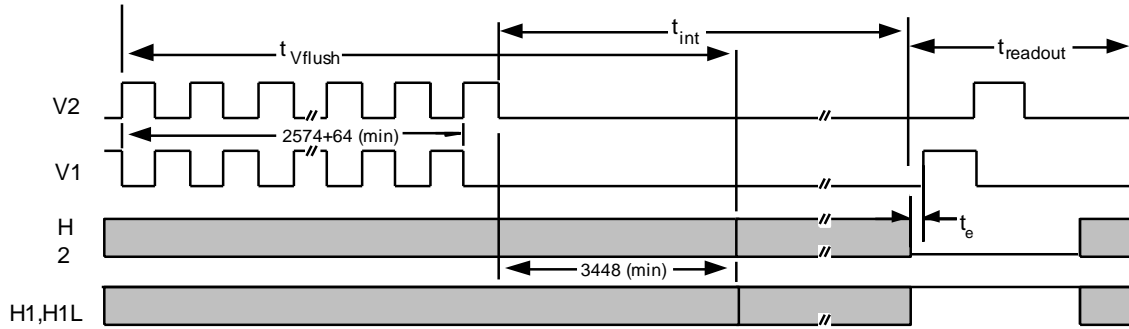


Figure 18: Power-up Flush Cycle



Storage and Handling

STORAGE CONDITIONS

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T _{ST}	-20	80	°C	1
Humidity	RH	5	90	%	2

Notes:

1. Storage toward the maximum temperature will accelerate color filter degradation.
2. T=25 °C. Excessive humidity will degrade MTTF.

ESD

1. This device contains limited protection against Electrostatic Discharge (ESD). ESD events may cause irreparable damage to a CCD image sensor either immediately or well after the ESD event occurred. Failure to protect the sensor from electrostatic discharge may affect device performance and reliability.
2. Devices should be handled in accordance with strict ESD procedures for Class 0 (<250V per JESD22 Human Body Model test), or Class A (<200V JESD22 Machine Model test) devices. Devices are shipped in static-safe containers and should only be handled at static-safe workstations.
3. See Application Note *Image Sensor Handling Best Practices* for proper handling and grounding procedures. This application note also contains workplace recommendations to minimize electrostatic discharge.
4. Store devices in containers made of electro-conductive materials.

COVER GLASS CARE AND CLEANLINESS

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided.
3. Improper cleaning of the cover glass may damage these devices. Refer to Application Note *Image Sensor Handling Best Practices*.

ENVIRONMENTAL EXPOSURE

1. Extremely bright light can potentially harm CCD image sensors. Do not expose to strong sunlight for long periods of time, as the color filters and/or microlenses may become discolored. In addition, long time exposures to a static high contrast scene should be avoided. Localized changes in response may occur from color filter/microlens aging. For Interline devices, refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible lighting Conditions*.
2. Exposure to temperatures exceeding maximum specified levels should be avoided for storage and operation, as device performance and reliability may be affected.
3. Avoid sudden temperature changes.
4. Exposure to excessive humidity may affect device characteristics and may alter device performance and reliability, and therefore should be avoided.
5. Avoid storage of the product in the presence of dust or corrosive agents or gases, as deterioration of lead solderability may occur. It is advised that the solderability of the device leads be assessed after an extended period of storage, over one year.

SOLDERING RECOMMENDATIONS

1. The soldering iron tip temperature is not to exceed 370 °C. Higher temperatures may alter device performance and reliability.
2. Flow soldering method is not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. Recommended method is by partial heating using a grounded 30 W soldering iron. Heat each pin for less than 2 seconds duration.



Mechanical Information

VISUAL MECHANICAL SPECIFICATIONS

Laser Mark

Item	Description
Device Name	KAF-8300CE, KAF-8300XE, or KAF-8300-AXC. (Multiple versions available) See ORDERING INFORMATION section of this document
Serial Number	nnn –a numeric field containing a maximum of three characters denoting a unique unit identifier for a device from the before mentioned production lot. The start of the sequence starts with "1". "001" is not a valid marking.

All markings shall be readable, consistent in size with no unusual debris left on the package.

Assembly/Package Integrity

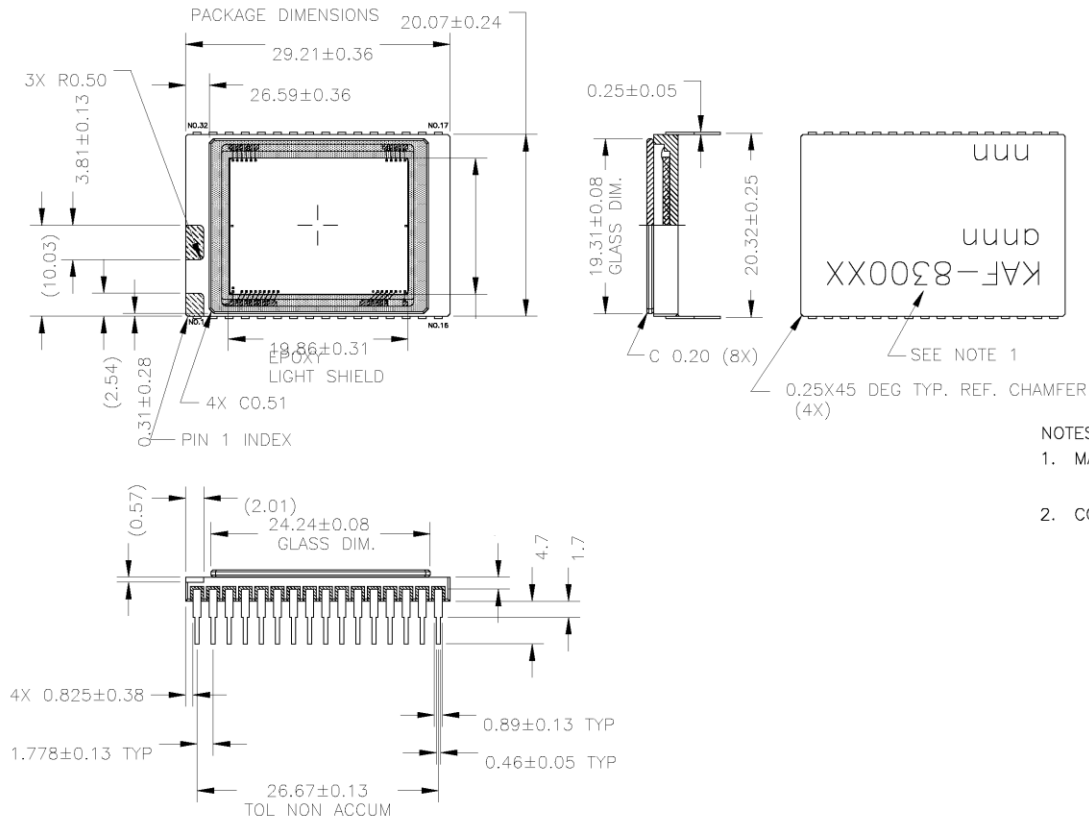
Criteria	Description
Cracks	None allowed
Corner and edge chip-outs	None – exceeding 0.020" (0.50 mm)
Chip-outs exposing buried metal traces	None allowed
Chip-outs, other	None allowed deeper than 50% of the ceramic layer thickness in which it resides
Scratches	None – that exceed 0.20" (0.50 mm) in the major dimension and are deeper than 50% of the ceramic layer thickness in which it resides.
Lead conditions	No bent, missing, damaged, or short leads. No lead cut-off burrs exceeding 0.005" (0.13 mm) in the dimension away from the lead.
Internal Appearance And Die Condition	Local Non-Uniformity: Local Non-Uniformity region (LNU) is allowed whose size is not greater than 200 um ² within the effective image area. Inspection equipment for these steps are performed using a microscope 7-50X and direct lighting (ring-light). LNU is described as a spot or streak that tends to change from light to dark in appearance as the operator rotates the part under angled lighting conditions. These non-uniformities are not visible or very hard to see under direct lighting. They tend to disappear or become much less visible under higher magnification. Conditions Other than LNU: No scratches, digs, contamination, marks, or blemishes that is attached to the die that touches 9 or more pixels in the effective image area. No loose contamination allowed when viewed at 7X and 50X magnification. No scratches, digs, contamination, marks, or blemishes greater than 10 µm are allowed on the bottom side of the cover glass region that is contained in or extends into the effective image area. Tools used to verify are 7X and 50X magnification.

Glass

Criteria	Description
Tilt	The reject condition is when the glass is incorrectly seated on the package or is not parallel to glass seal area. ("parallel" is defined as 0.25 mm maximum end to end).
Seal	Glass seal must be greater than 50% of the width of the epoxy bond line and must not extend over the ceramic package.
Alignment	There are 4 "+" fiducials on the corners the die that must not be covered by the epoxy light shield. The 4 "+" marks must be in total view when the lid is placed looking directly down on the device with a microscope. All 4 "+" alignment marks are required to be visible in their entirety with a zero clearance tolerance.
Chips	None allowed.
Appearance	No fogged cover allowed.
Contamination	No immobile scratches, digs, contamination, marks, or blemishes are allowed on the cover glass region that is contained in or extends into the effective image area. Within the effective image area, the limit for such conditions is 10um or less. This criterion pertains to either the top or the bottom glass surface. Tools used to verify are 7X and 50X magnification.



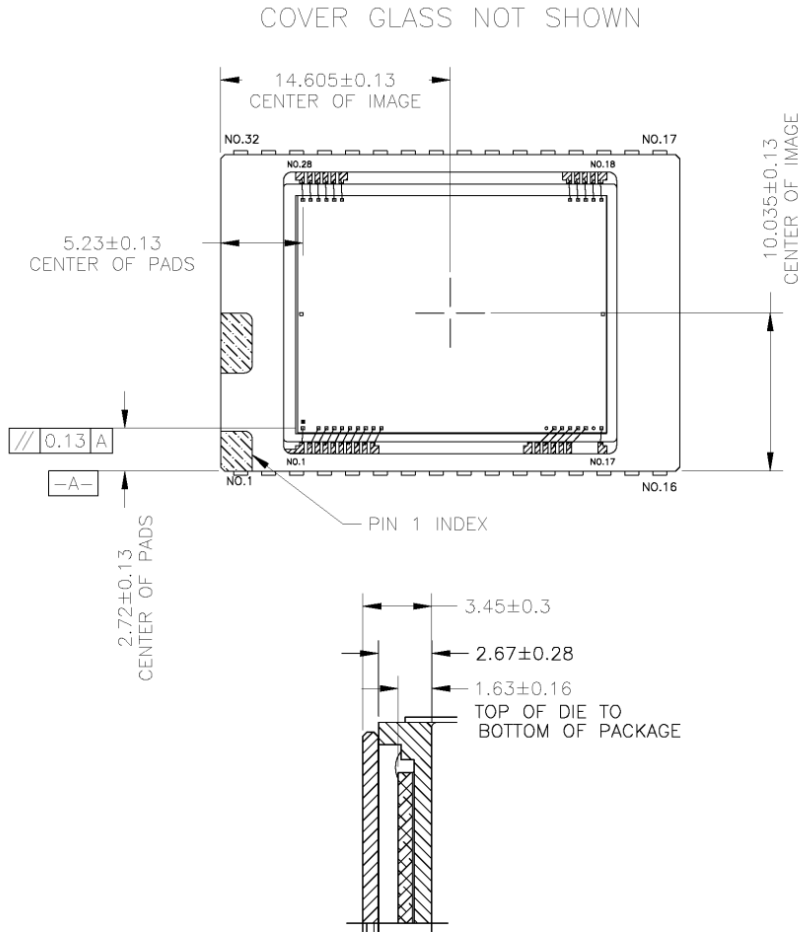
COMPLETED ASSEMBLY



NOTES:

- MARKING CODE:
 ann IS PRODUCTION RUN NUMBER.
 nnn IS SERIAL NUMBER
- COVER GLASS SPECIFICATIONS:
 THICKNESS 0.76±0.05
 Nd 1.5231 @ 588nm
 DISPERSION 0.0096

Figure 19: Completed Assembly (1 of 2)



- NOTES:
1. CENTER OF IMAGE AREA IS OFFSET FROM CENTER OF PACKAGE BY (0.00,0.00)MM NOMINAL.
 2. ANGULAR SPECIFICATION: DIE TO PACKAGE < 1DEGREE.

Figure 20: Completed Assembly (2 of 2)



COVER GLASS

Clear Cover Glass, AR Coated (both sides) - Specification

1. Scratch and dig: 10 micron max
2. Substrate material Schott D263T eco or equivalent
3. Multilayer anti-reflective coating

Wavelength	Total Reflectance
420-450	≤ 2%
450-630	≤ 1%
630-680	≤ 2%

Clear Cover Glass – Specification

1. Scratch and dig: 10 micron max
2. Substrate material Schott D263T eco or equivalent

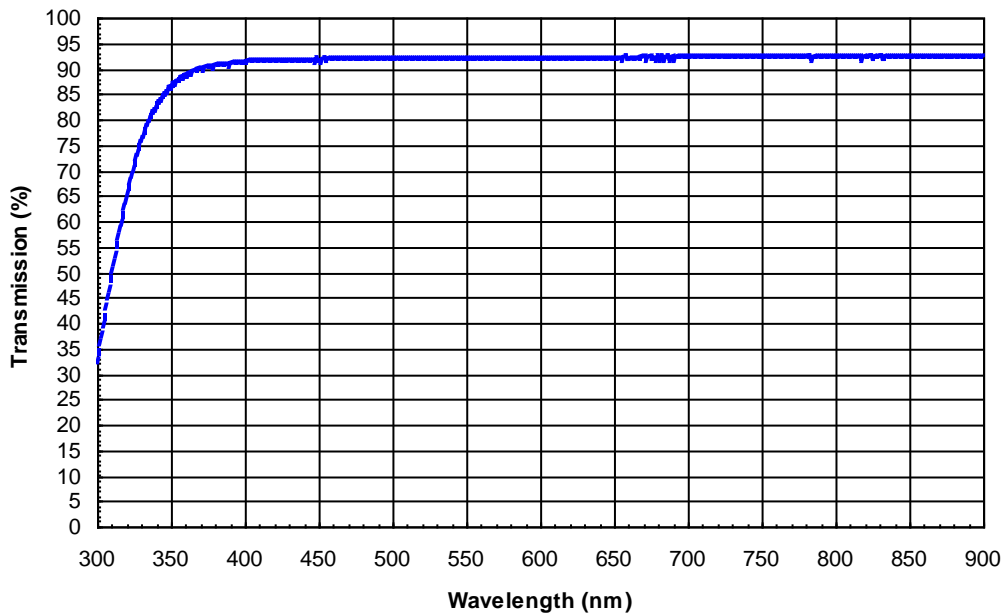


Figure 21: Clear Cover Glass Transmission, Typical



Quality Assurance and Reliability

QUALITY AND RELIABILITY

All image sensors conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and visual inspection and electrical testing at key points of the manufacturing process, using industry standard methods. Information concerning the quality assurance and reliability testing procedures and results are available from ON Semiconductor upon request. For further information refer to Application Note *Quality and Reliability*.

REPLACEMENT

All devices are warranted against failure in accordance with the *Terms of Sale*. Devices that fail due to mechanical and electrical damage caused by the customer will not be replaced.

LIABILITY OF THE SUPPLIER

A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer. Product liability is limited to the cost of the defective item, as defined in the *Terms of Sale*.

LIABILITY OF THE CUSTOMER

Damage from mishandling (scratches or breakage), electrostatic discharge (ESD), or other electrical misuse of the device beyond the stated operating or storage limits, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

TEST DATA RETENTION

Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

MECHANICAL

The device assembly drawing is provided as a reference.

ON Semiconductor reserves the right to change any information contained herein without notice. All information furnished by ON Semiconductor is believed to be accurate.

Life Support Applications Policy

ON Semiconductor image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of ON Semiconductor.




Revision Changes

MTD/PS-0996

Revision Number	Description of Changes
1.0	<ul style="list-style-type: none"> Initial Release.
2.0	<ul style="list-style-type: none"> Add monochrome versions and the allowance of differentiating high volume packing.
3.0	<ul style="list-style-type: none"> Reference to Web Site noted on Ordering Information page. Added references to Application Note Image Sensor Handling and Best Practices. Removed descriptions and drawings related to high level packing.
4.0	<ul style="list-style-type: none"> Corrected Active Image Size to 17.96mm x 13.52mm
5.0	<ul style="list-style-type: none"> Changed Sample Plan to Verification Plan. Added new revision of completed assembly drawing
5.1	<ul style="list-style-type: none"> Corrected units in table in Capacitance Equivalent Circuit section.
5.2	<ul style="list-style-type: none"> Corrected Evaluation Board Kit Name to KEK-4H0471-KAF- 8300-12-28
5.3	<ul style="list-style-type: none"> Changed cover glass material to D263T eco or equivalent
5.4	<ul style="list-style-type: none"> Changed units for H1, H2 Setup Time from ms to μs

PS-0029

Revision Number	Description of Changes
1.0	<ul style="list-style-type: none"> Initial release with new document number, updated branding and document template. Updated <i>Storage and Handling</i> and <i>Quality Assurance and Reliability</i> sections. Updated Imaging Performance tables.
1.1	<ul style="list-style-type: none"> Updated branding

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